Design Decisions:

1. LI instruction words are grabbed on the same clock cycle. The LI op-code triggers another memory read. This was done to reduce the complexity determining how each stage should execute for a given instruction; every instruction is ready for execution in one clock cycle. It also reduces the complexity of the jump and squash instructions.
2. Dependencies were handled through the use of flags that made each affected stage halt.
3. Each stage was given the same size memory. This was done to aid in the design/testing process.
4. The ALU from Alex’s Project 2 was used because it had simple inputs and outputs and it was simpler to use it than to write a new one.

Design process

1. Hardware was built for instructions that utilized the ALU first. This was done because it allowed for testing the largest number of instructions before extra hardware and logic were added.
2. Control logic and hardware for every instruction besides JZ and SZ was added next. Control logic for each instruction was added sequentially with testing in between each one.
3. SZ was done because it had the simplest implementation. It just made HiZ propagate through the rest of the stages.
4. JZ was done after SZ because it was a little more complicated. The hardware and logic designed for SZ helped with JZ.
5. Logic to handle dependencies was added last. This was done because we wanted to know the processor worked without any problems.

Testing Process

1. The hardware and logic for each instruction was tested as it was designed. This made sure each instruction could execute before having to run a test program.
2. Once the hardware and logic were confirmed to work independent for each instruction, a simple test program was executed. This program did not have dependencies and only checked that there were no problems executing multiple instructions.
3. As the logic for handling dependencies was developed, smll programs of 2-3 instructions were used to test it.
4. A complete program which hits every line of Verilog was developed and used to verify correctness.